**Digital System Design**

**Lab01**

**Spring 2025**

Submitted by: **Mohsin Sajjad**

Registration No: **22pwsce2149**

Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”



Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (16 02, 2025)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

# LAB No 1

**INTRODUCTION TO MODELSIM AND GATE LEVEL MODELING**

**Objectives:**

Introduction to MODELSIM

**Software used:**

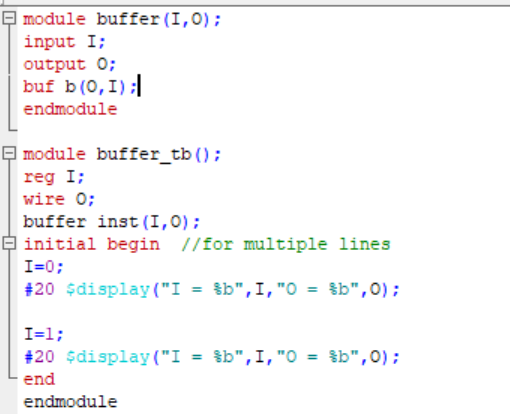
MODELSIM

**MODELSIM:**

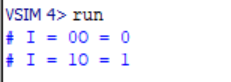
MODELSIM is a simulator which can be used for the simulations of both VHDL and Verilog HDL. It has the following interface.

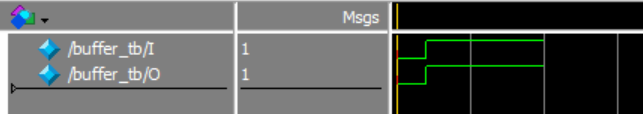
**TASKS:**1. Implement a buffer at the gate level.

**CODE:**

****

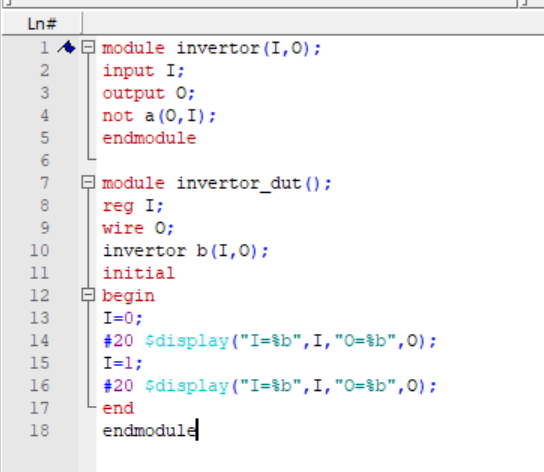
**Truth table:**

****

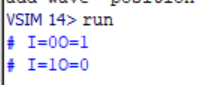
**Wave output:  
**

2. Implement an inverter at the gate level.

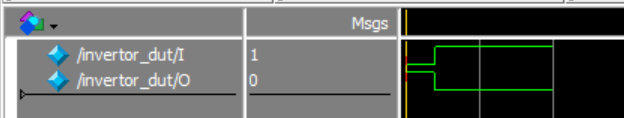
Code:



Truth Table:

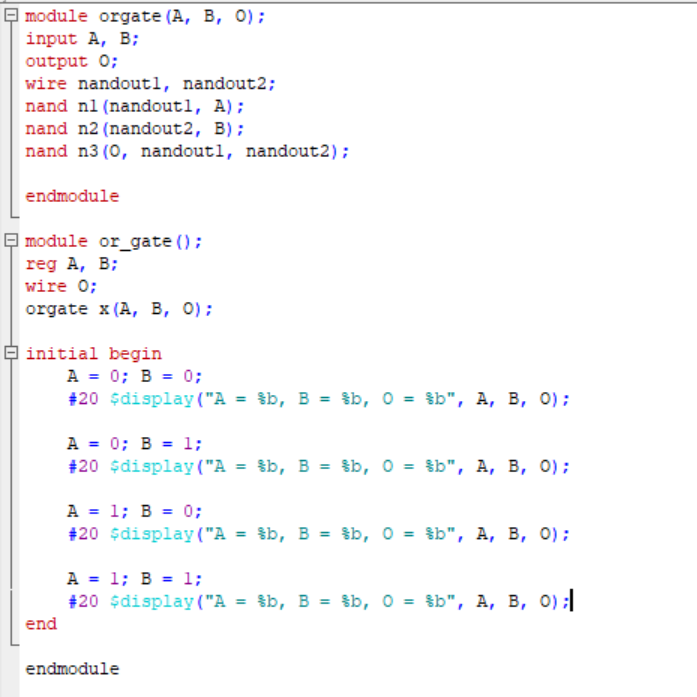


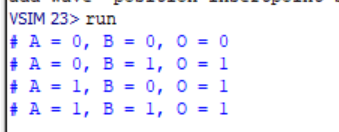
Wave output:



3. Implement an OR gate using a NAND gates.

Code:





Wave output:

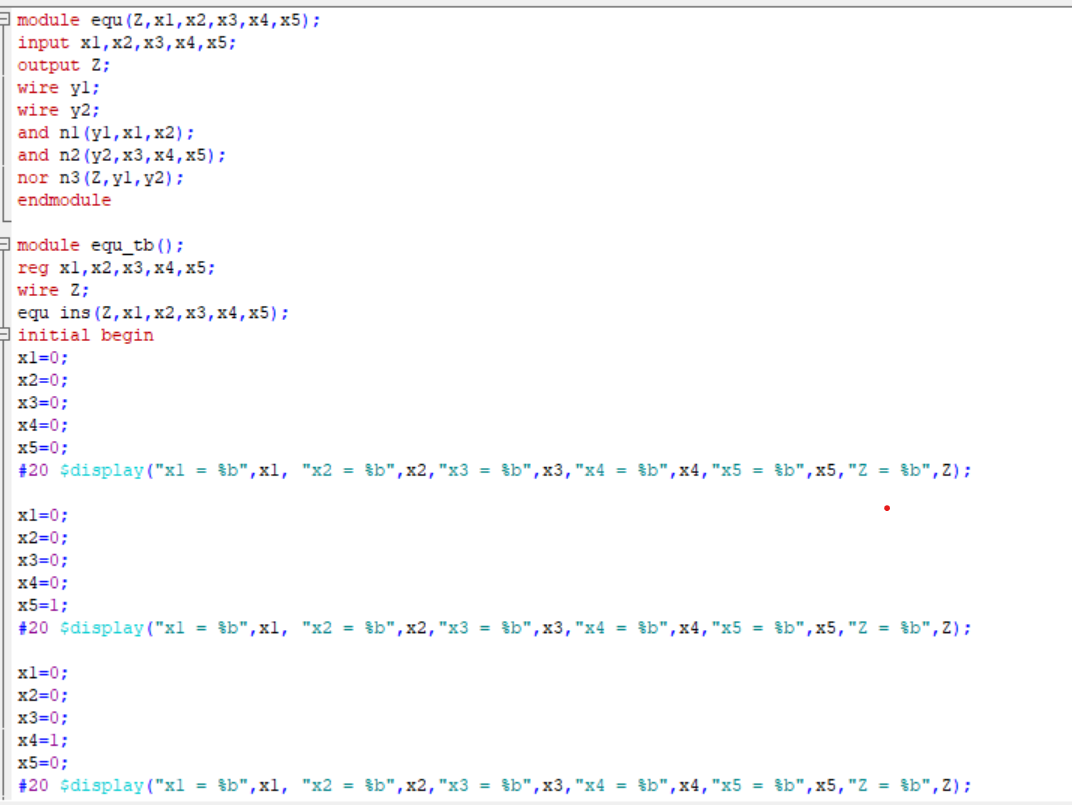


4. Implement the following equation where z is output and x1, x2, x3, x4, and x5 are inputs of the circuit.

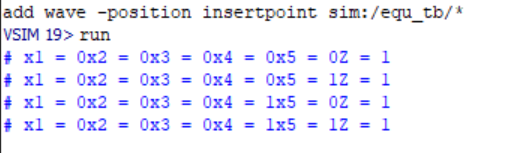
z = ( y1 + y2 )’

y1 = x1.x2

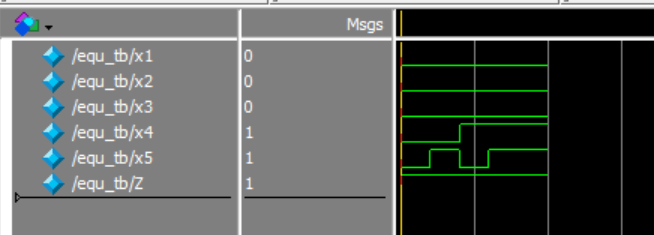
y2 = (x3.x4.x5)



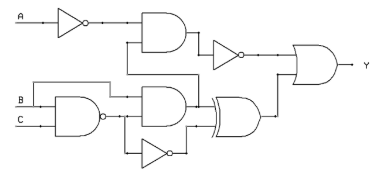
Truth Table:

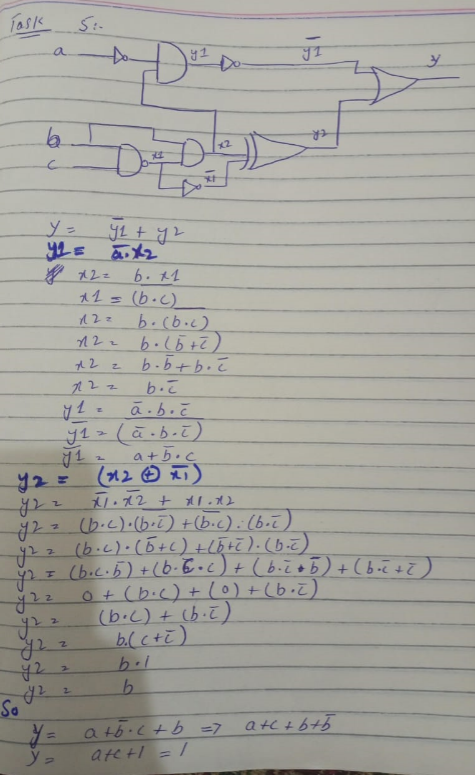


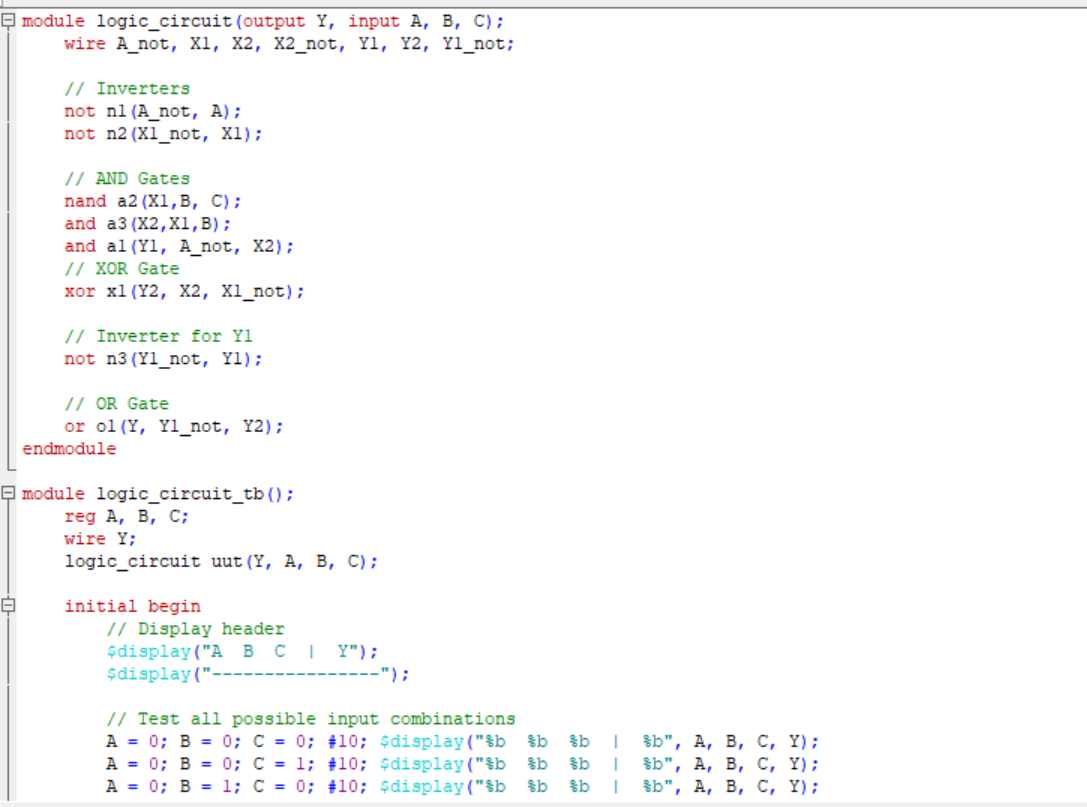
Wave output:

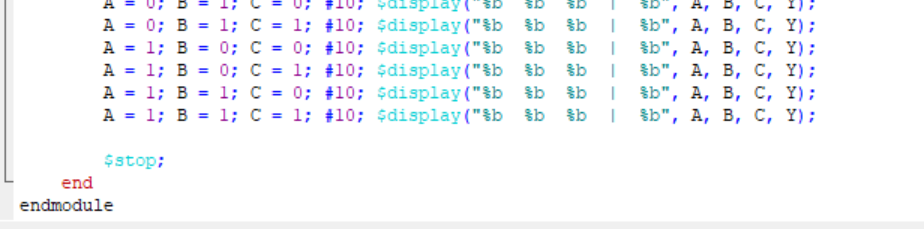


5.

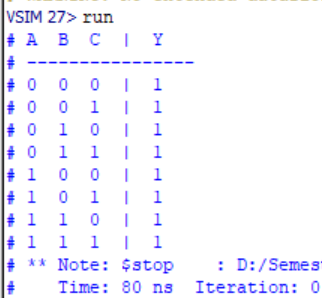








**Truth table:**



Wave output:

